

應用 s 域右半平面極點製作振盪器

Application of the s-domain Right-Half-Plane Poles to Construct Oscillator

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摘要

寄生電容在電子電路中是常見卻難以免除的現象，製作高頻振盪器時，寄生電容又是必需考量的因素之一。散佈在振盪電路各處的寄生電容可能造成振盪器迴路增益小於 1 而無法振盪，因此本文提出一個方法，既然寄生電容必定存在於振盪電路之中，那可否改變振盪器電路結構來彌補寄生電容對振盪器所造成的影響，使得振盪器能夠在寄生電容的影響下順利振盪。本文所提出的振盪器與其它振盪器最大的不同點在於本電路具有極點座落於 s 域右半平面的二階轉移函數。這個二階轉移函數可彌補電路中寄生電容的影響進而使得振盪電路能夠順利振盪。

關鍵詞：極點，振盪器，運算轉導放大器，電流回授放大器

Abstract

Parasitic capacitances in the electronic circuits are often observable, but are difficult to remove it. On the process of making high-frequency oscillators, parasitic capacitances as one of the major factors have to be put into consideration. Parasitic capacitances scattered in oscillator circuits may cause the loop gain of the oscillator at a value smaller than 1, unable to oscillate. In this study, we give a proposal that since parasitic capacitances always exist in the oscillator circuit, if the structure of the oscillator circuit would change, the impact of parasitic capacitances may be therefore compensated. Consequently, the oscillator, even under the influence of parasitic capacitances, can still oscillate in a smooth way. In this study, the feature of the proposed oscillator distinctive from other oscillators is that the circuit has poles located at the second-order transfer function in the right half s-plane. The second-order transfer function can make compensation for the impact of the parasitic capacitances in the circuit, enabling the oscillation circuit to oscillate smoothly.

Keywords: pole, oscillators, operational transconductance amplifiers (OTA), current feedback amplifier (CFA)

I. INTRODUCTION

In recent years, a current-mode circuit has been widely noticeable for precision characteristics and low power consumption [1] because of its wider bandwidth, higher slew rate, and larger linear dynamic range. Currently, many studies on oscillators [2-4] in the design of current-mode circuits have already proposed. In the oscillator theory [5], the second-order oscillator needs to place the poles at exact locations on the imaginary axis in the s-plane before a smooth oscillation. If the poles are placed at the left of the imaginary axis in the s-plane, because the output will decrease as the time increases, the oscillation cannot be carried.

Parasitic capacitances in the electronic circuit are frequently seen. There are some studies published [6] in an effort to improve the impact of parasitic capacitances in electronic circuits. Parasitic capacitances scattered in the oscillator may cause the loop gain insufficiency in the oscillation circuit at high frequencies, resulting a failure of oscillation. In this study, we propose a way to make improvement for insufficient loop gain caused by parasitic capacitances. In application of active components and an external bias circuit to construct two poles, close to the second-order function at the right half s-plane; the poles in the right half s-plane can cause the value of a loop gain greater than 1, whose characteristics is used to compensate

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for the oscillator circuit with a loop gain smaller than 1 because of parasitic capacitances.

In this study, two operational transconductance amplifiers (OTA) are used to design a second-order function with poles in the right half s-plane, and then two current feedback amplifiers (CFA) make a practical second-order oscillator with two poles located in the right half s-plane. Under the impact of parasitic capacitances, the oscillator is still able to restart because of the poles located at the right half s-plane.

II. CIRCUIT DESCRIPTION

In view of methodology proposed in this paper, firstly, we need to build a second-order function with two poles located at the right half s-plane. Two OTA components are applied to construct a second-order function with poles located in the right half s-plane. The symbol of OTA component is shown in Figure 1.

Input and output relationship of OTA can be denoted by Eq. (1):

$$I_o = g_m \times (v_+ - v_-) \quad (1)$$

With two OTA components, the second-order oscillator circuit is constructed, shown as Figure 2, which is modified from the quadrature oscillator [7-8].

From Figure 2 circuit, we may deduct a second-order function with poles located at the right-half plane in s-domain, as shown in Eq. (2):

$$s^2 - \frac{g_{m1}}{C_1} s + \frac{g_{m1} \cdot g_{m2}}{C_1 C_2} = 0 \quad (2)$$

The poles deduced by Eq. (2) second-order function is denoted as Eq. (3):

$$s_p = \frac{g_{m1}}{2C_1} \pm \frac{1}{2} \sqrt{\left(\frac{g_{m1}}{C_1}\right)^2 - 4 \frac{g_{m1} g_{m2}}{C_1 C_2}} \quad (3)$$

From Eq. (3), it is known that s_p are the poles located at the right half s-plane. In dealing with the problem that loop gain smaller than 1 because of parasitic capacitances, this paper proposes a method to make up the insufficiency by the help of the application of the characteristic of the poles in the right half s-plane.

Next, we chose CFAs to make a practical oscillation circuit with poles located in the right-half s-plane; CFA uses a commercial IC AD844 for Analog Devices, whose simplified schematic were constituted by the BJT elements, as shown in Figure 3 [9].

A CFA is equivalent to a second-generation current conveyor (CCII+) with its output is cascaded to a voltage buffer, in which the symbol of CCII+ circuit component is shown in Figure 4.

The characteristics of the input and the output of the CCII+, are given in Eq. (4):

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix} \quad (4)$$

In case, CCII+ and a voltage buffer are in combination at output, which can constitute a CFA component; the practical component is the IC AD844. However, each actual component is not capable of achieving its ideal circuit characteristics; naturally, IC AD844 can not be excepted. Figure 5 shows the AD844 non-ideal characteristics equivalent diagram [10]. At the later part, we will give a description of a practical oscillation

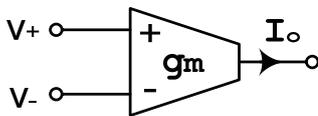


Fig. 1 Symbol of the Operational Transconductance Amplifier (OTA)

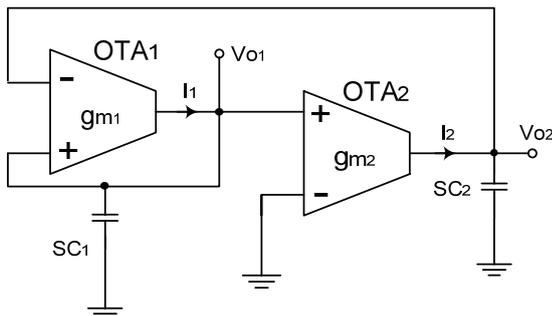


Fig. 2 Second-order Oscillator made by two OTAs

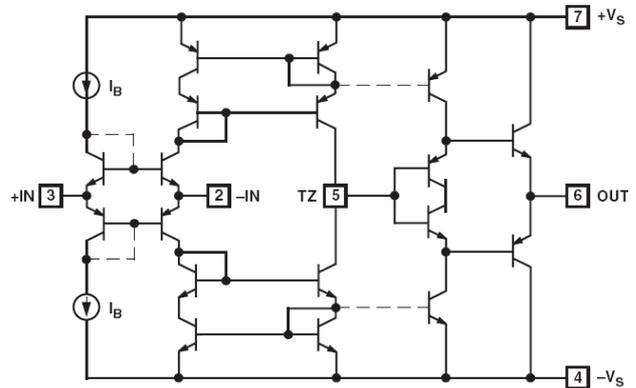


Fig. 3 AD844 Simplified schematic

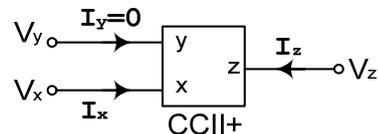


Fig. 4 CCII+ circuit symbol

circuit in the experiment, together in consideration with the non-ideal characteristics in Figure 5.

The CFA active component would be replaced by IC AD844; afterwards, the physical circuit can be expressed in Figure 6.

Figure 6 shows the second-order function of the oscillator circuit, which can be denoted by Eq. (5):

$$s^2 - \frac{C_3}{R_2 C_2 (C_1 + C_3)} s + \frac{1}{R_1 R_2 C_2 (C_1 + C_3)} = 0 \quad (5)$$

Figure 6 shows the oscillation circuit having the frequency f_0 , which can be determined by [11]:

$$f_0 = \frac{1}{4\pi} \sqrt{\frac{4}{R_1 R_2 C_2 (C_1 + C_3)} - \left[\frac{C_3}{R_2 C_2 (C_1 + C_3)} \right]^2} \quad (6)$$

In the oscillator theory, equation (5) shows in the second-order function, in case the capacitor C_3 is equal to 0, the poles of an oscillator would be the conjugate imaginary roots on the imaginary axis of the s-plane; the oscillation frequency would be $f_0 = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$. In a practical circuit experiment, in case C_3 is not zero, the second-order function will provide two poles located in the right half s-plane, which can be used to compensate for insufficient circuit gains of the circuit oscillating at high frequencies, thus keeping the oscillator in oscillation at high frequencies. At this point, the oscillation frequency is denoted as Eq. (6).

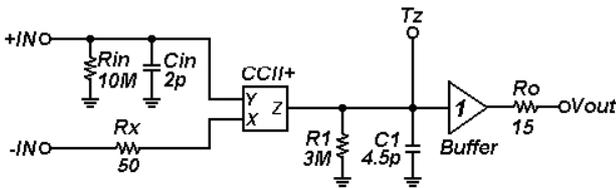


Fig. 5 AD844 non-ideal characteristics equivalent diagram

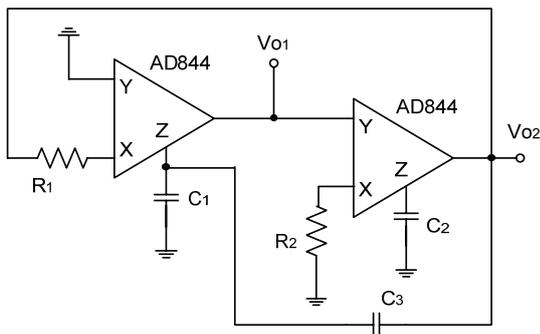


Fig. 6 Second-order oscillator with poles located in the right half s-plane

III. EXPERIMENTAL RESULTS

If the non-ideal characteristics of the AD844 would be considered in Figure 5, the capacitance impact of the T_z terminal and the non-inverting terminal in Figure 6 can put together with the value of actual electronic components in calculation. The combination of the actual electronic component and capacitance impact in Figure 6 should be $R_1 = 10.27 \text{ K}\Omega$, $R_2 = 2.98 \text{ K}\Omega$, $C_1 = 56.7 \text{ pF}$, $C_2 = 26.2 \text{ pF}$, $C_3 = 12.1 \text{ pF}$.

If the above component is produced as the circuit in Figure 6 and then is measured with an oscilloscope GWinstek GDS-1042, as shown in Figure 7; the oscillation frequency of the oscilloscope would be 646.38 KHz.

If the component value should be put into Eq. (6), it can obtain $f_0 = 653.47 \text{ KHz}$ with a deviation of 1.09%. In addition, Figure 8 shows FFT analysis of oscillation waveform was displayed with an oscilloscope. Figure 8 show the frequency spectrum of the voltage output waveforms.

Eq. (5) shows if C_3 in Figure 6 is removed, the poles at this time will just fall on the imaginary axis of the s-plane, which should be able to produce a waveform and its oscillation frequency should be $f_0 = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$.

However, the actual measurement of the oscillator with an oscilloscope is not the case. In the practical oscillator experiment, if C_3 in Figure 6 is to be removed, oscillation waveforms can not be produced by the oscillation circuit, shown in Figure 9.

IV. CONCLUSIONS

Parasitic capacitances scattered around the oscillator circuit may cause the circuit loop gain smaller less than 1, unable to have smooth oscillations. This paper gives a proposal to have compensation for insufficient loop gains caused by parasitic capacitances to deal with the oscillation problem. This method is designed to construct a second-order function with poles located in the right half s-plane. When the poles are located in the right half s-plane,

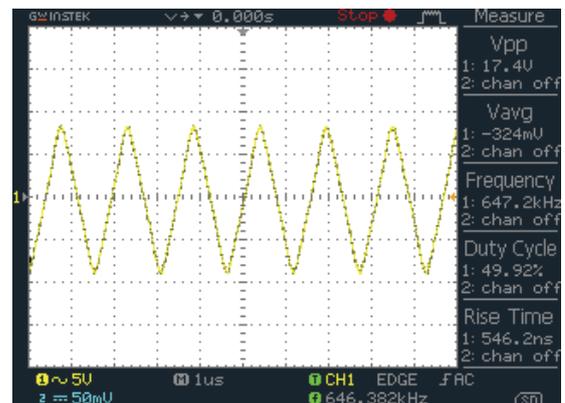


Fig. 7 $C_3 \neq 0$, the oscillation waveform displayed with an oscilloscope

the loop gain of the oscillator is greater than 1. The characteristic can be properly used to make up for insufficient oscillation circuit loop gain, smaller than 1, caused by parasitic capacitances. When the pole goes to more extreme in the right half s-plane, the loop gain of oscillation circuit will diverge more seriously. This paper aims the loop gain caused by the poles in the right half s-

plane may almost offset the insufficiency caused by parasitic capacitances. Therefore, there is a need for poles located in the right half s-plane, trying to get closer to the imaginary axis so as to offset the impact of parasitic capacitances. The proposed method can not only improve the impact caused by the parasitic capacitances, but also improve other decreased loop gains on the production process of the oscillation circuit. In addition, the probability of success to make high-frequency oscillation circuits can be further enhanced.

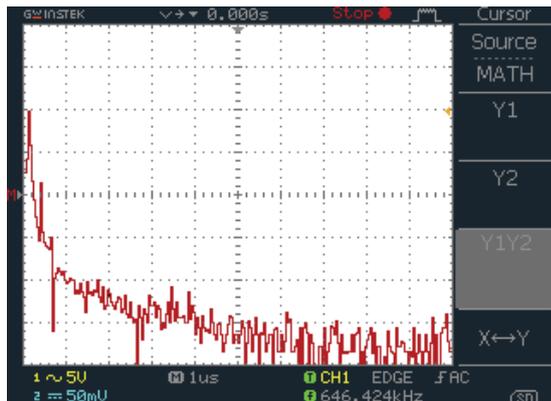


Fig. 8 FFT analysis of oscillation waveforms

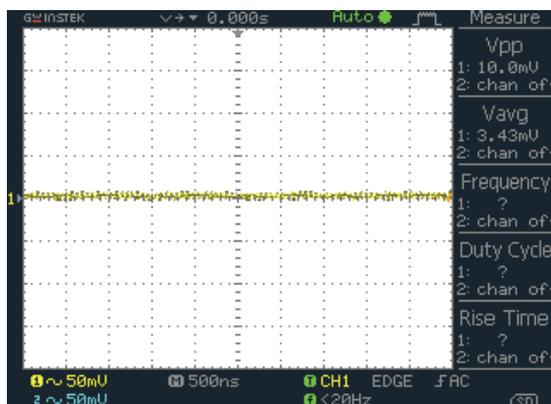


Fig. 9 $C_3=0$, oscillation waveforms displayed with an oscilloscope

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