以電流式切換電容電路實踐類比信號取樣延遲電路
An Analog Signal Sample Delay Circuit Based on Current Mode Switched-Capacitor Circuit

侯俊禮* 馮健維 洪君維
Chun-Li Hou*, Jian-Wei Feng, Jiun-Wei Horng

摘要

本文提出一個電流式電路為架構的切換式電容電路，電流回授放大器 (CFA) 的高迴轉率，高操作頻率以及高動態範圍的特性可以被用來取代傳統的電壓式運算放大器。本文提出以切換式電容電路做一個信號採樣及維持延遲電路並與無延遲採樣與維持電路組合來設計出一個零階維持電路 (ZOH)。

關鍵詞：電流回授放大器 (CFA)，零階維持電路 (ZOH)，切換式電容電路

Abstract

This paper describes a current-mode switched capacitor circuit. The high performance of CFA (high slew rate, high operating speed, and wider dynamic range) is used to replace tradition voltage operational amplifiers. We present using a current mode SC circuit to design a delay S/H circuit and use this circuit with a non delay S/H circuit to design a ZOH circuit.

Keywords: current feedback amplifier (CFA), zero order hold circuit (ZOH), switched-capacitor circuit (SC)

I. INTRODUCTION

The current-mode circuits have been receiving much attention because of their potential advantages: higher bandwidth capability, less circuit complexity, higher operating speed, wider dynamic range, and the simpler circuitry [1]. The bandwidths of voltage operational amplifiers (VOAs) are fixed, and the slew rate is determined by the ratio of a quiescent current to the compensation capacitor or load capacitor [2].

The CFAs exhibit the potentiality of extended operating bandwidths and relatively large values of slew rates compared to the conventional voltage-feedback amplifiers. Note that a CFA is equivalent to a plus-type second-generation current conveyor (CCII) with a voltage follower [3]. The current feedback amplifier (CFA) is a four port building block frequency in analog signal processing circuits. A current feedback amplifier AD844 was provided by Analog Devices Inc [4-7].

Switched-Capacitor (SC) circuits achieve high precision and low distortion. The precision of a SC circuits mainly depends on capacitor matching that can be controlled very well (less than 0.1% error is possible with good layout technique), the circuit performance is therefore insensitive to process variation.

II. CIRCUIT DESCRIPTION

An ideal CFA is characterized by

$$\begin{bmatrix} I_y \\ V_x \\ I_z \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix} \quad (1)$$

The circuit symbol of the CFA is shown in Fig. 1, the non-ideal equivalent circuit of the CFOA is shown in Fig. 2, the typical data sheet values of the various parasitic for bipolar CFA such as AD844, $R_X^{'}$=50 Ω, $R_Y^{'}$=2 MΩ, $C_Z^{'}$=5.5 pF, $R_Z^{'}$=3 MΩ.

A current-mode Switched-Capacitor non-inverting voltage amplifier is shown in Fig. 3. $V_0^*(t) = v^o(t) + v^e(t)$, $V_0^*(t)$ is output sample signal, $v^o(t)$ is signal during ϕ_1 on and $v^e(t)$ is signal during ϕ_2 on. Using standard notation, the port relations of a CCII can be characterized by $v_x = v_y$, $i_z = \pm i_x$ and $i_y = 0$, during the switch ϕ_1 is on and time $t = (n-1)T$ to $t = (n-1/2)T$ the transfer functions can be expressed as

$$V_{C1}^o(n-1)T = V_{in}^o(n-1)T \quad (2)$$

中原大學電子工程學系
*Corresponding author. E-mail: clhou@cycu.edu.tw
Department of Electronic Engineering, Chung Yuan Christian University, Chung-Li, Taiwan, R.O.C
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And

$$V_{C2}^{o}(n-1)T = V_{out}^{o}(n-1)T = 0 \tag{3}$$

When ϕ_2 in

$$V_{out}^{e}(n-\frac{1}{2})T = \left(\frac{C_1}{C_2}\right)V_{in}^{o}(n-1)T \tag{4}$$

The z-domain transfer function as given below

$$V_{out}^{e}(z) = \left(\frac{C_1}{C_2}\right)z^{-1/2}V_{in}^{o}(z) \tag{5}$$

In the last ϕ_2 clock the input signal is still $v_{in}^{o}(n-1)T$, Eq. 5 can be written as

$$V_{out}^{e}(z) = \left(\frac{C_1}{C_2}\right)z^{-1}V_{in}^{e}(z) \tag{6}$$

An inverting current-mode Switched-Capacitor voltage amplifier is shown in Fig. 4. The transfer functions can be expressed as

$$V_{out}^{e}(n-\frac{1}{2})T = -\left(\frac{C_1}{C_2}\right)V_{in}^{o}(n-\frac{1}{2})T \tag{7}$$

The z-domain transfer function as given below

$$V_{out}^{e}(z) = -\left(\frac{C_1}{C_2}\right)V_{in}^{e}(z) \tag{8}$$

This paper uses non-inverting voltage amplifier and inverting voltage amplifier to achieve a signal sampled and delay circuit.

III. SIMULATION

Experiments and simulations were carried out to demonstrate the feasibility of the proposed circuits. The CFA were implemented using AD844s. HSPICE is used to simulate the non-inverting voltage amplifier. The simulation result is shown in Fig. 5. In the Fig. 5

$$\text{the output voltage delay time} = (T_{L1} - T_{H2})/2 \tag{9}$$

and

$$\text{hold time} = (T_{L2} - T_{H1})/2 \tag{10}$$

$T_{L1} + T_{H1} = T_1$, $T_{L2} + T_{H2} = T_2$.

The sample clock is shown in Fig. 6(a), the switch is a complementary switch shown in Fig. 6(b), the complementary switch is used to reduce the on-resistance of the switch. In this paper use the sample delay to achieve a zero-order hold (ZOH) circuit, the ZOH input-output relation in the Laplace domain is written

$$H(s) = \frac{1-e^{-TS}}{s}E^{*}(s) \tag{11}$$

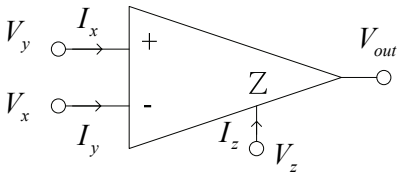

Fig. 1 Circuit symbol of CFA

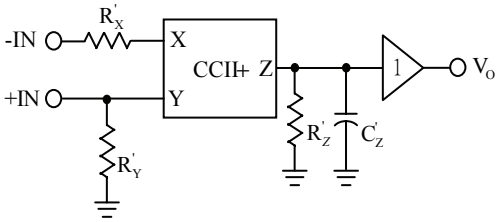

Fig. 2 Non ideal equivalent circuit of the CFA

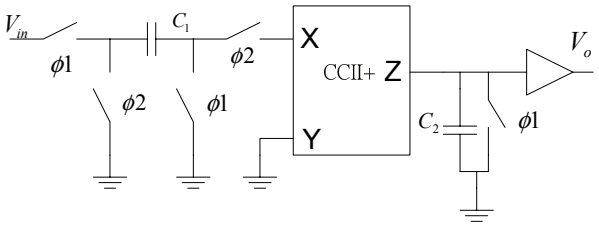

Fig. 3 Current-mode switched-capacitor non-inverting voltage amplifier

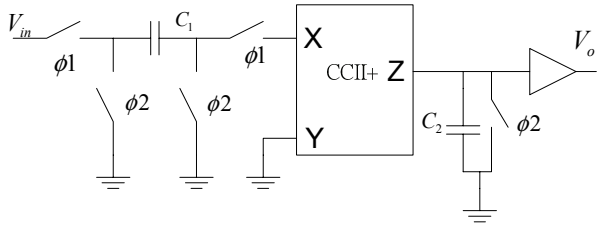

Fig. 4 Current-mode switched-capacitor inverting voltage amplifier

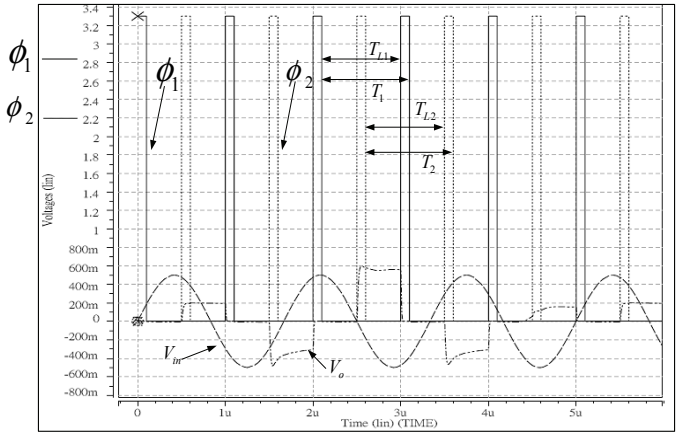

Fig. 5 The simulation result of non-inverting voltage amplifier

In the time domain, the relation is simply

$$h(t) = et(kT+) \text{ for } \quad kT \le t < (k+1)T \tag{12}$$

The ZOH structure is shown in Fig. 7.

The ZOH structure is achieve by Fig. 8,

$$V_{o1} = -V_{in}^{*}(t),\ V_{o2} = V_{in}^{*}(t-T),\ V_{o3} = -(V_{o1} + V_{o2}),$$
$$V_{o3} = (V_{in}^{*}(t) - V_{in}^{*}(t-T)) \tag{13}$$

The S-domain transfer function as given below

$$V_{O3}(S) = (1 - e^{-TS})V_{in}^{*}(S) \tag{14}$$

$$V_{OZ}(S) = \frac{1 - e^{-TS}}{s} V_{in}^{*}(S) \tag{15}$$

The simulation signal result of the circuit uses 1 MHz sinusoidal input and the output signal of the integrator is shown in Fig. 9. The charging time and holding time can be changed by shifting the sample signal. Because the AD844 is not ideal CFA, The transfer of electric charge from sample capacitor from load capacitor have lossy. Apparently, we can base on Eq. (6) and Eq. (8) to compensate the electric charge loss in terms of the ration increment between sample capacitor and load capacitor. In this simulation C1=12 pF, C2=5 pF, C3=12 pF, C4=5 pF. Sample capacitor voltage and v_{out} are shown in Fig. 10 and Fig. 11.

IV. CONCLUSION

A current-mode switched capacitor circuit is presented in this paper. This circuit replacing the traditional voltage-mode OP AMP by CFA. A non-delay signal and a inverted delay signal were used to building a ZOH block. The output signal of ZOH can be controlled easily by two sample clocks. The circuit structure in this paper is simple. The use of current-mode active element provides switched-capacitor circuit faster operation speed.

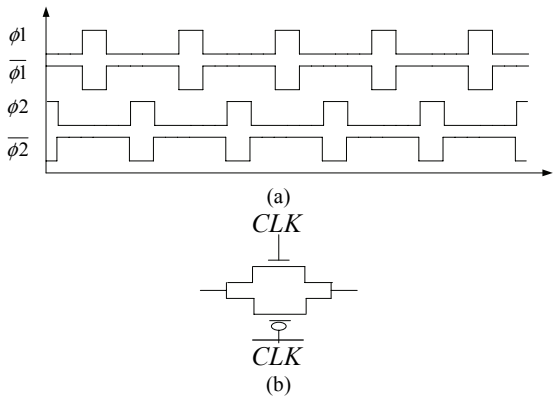

Fig. 6 (a) The sample clock, (b) sample switch

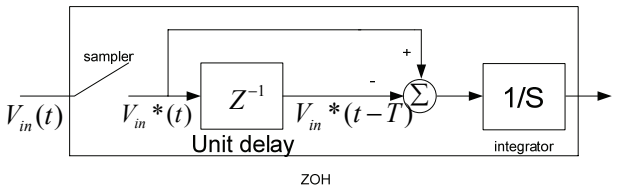

Fig. 7 The structure of zero-order hold

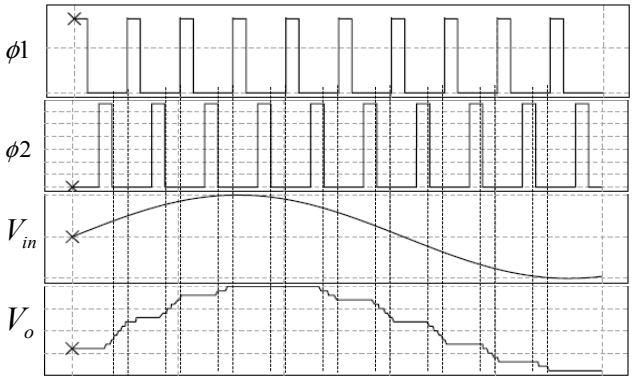

Fig. 9 The simulation result of zero-order hold circuit

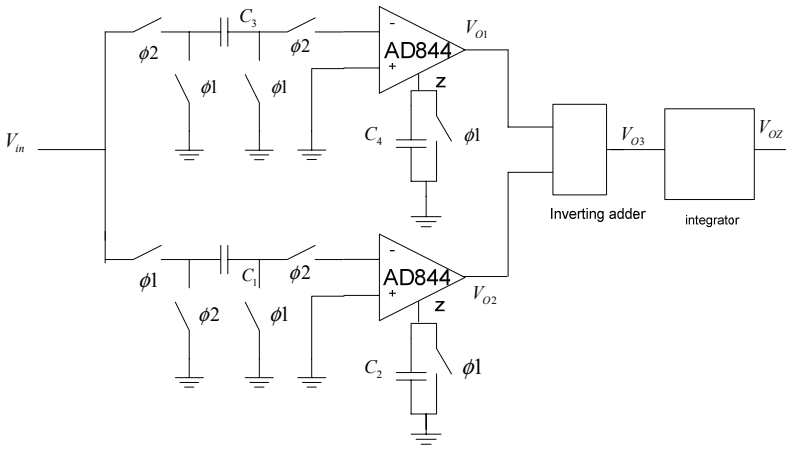

Fig. 8 The circuit of zero-order hold

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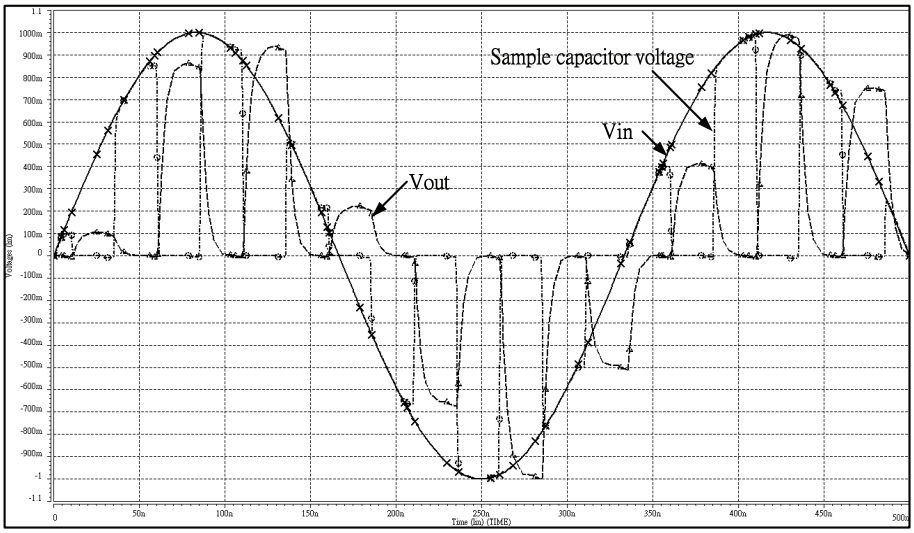

Fig. 10 The compare of sample capacitor voltage and vout in delay S/H unit

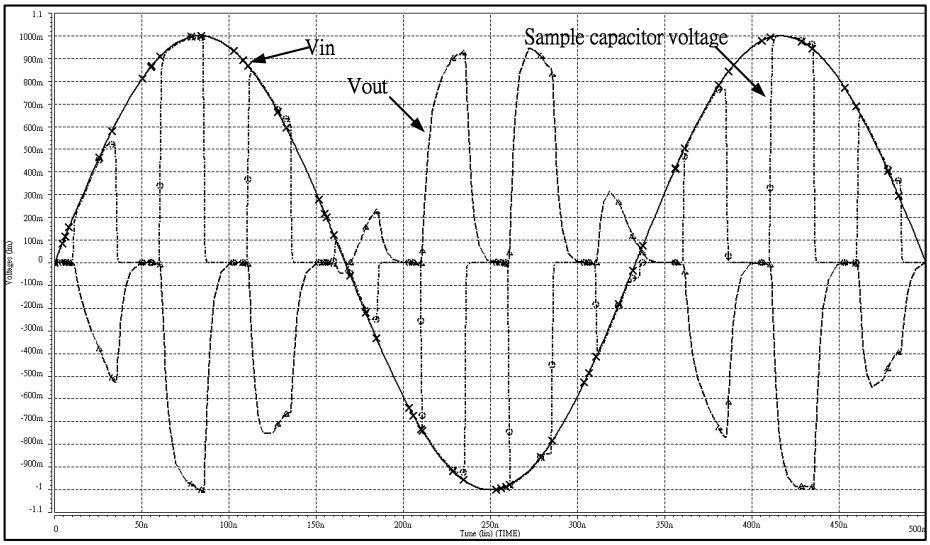

Fig. 11 The compare of sample capacitor voltage and vout in non delay S/H unit