應用於音源系統的自動增益控制
The Application of Automatic Gain Control to Audio System

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摘要

本論文中，簡短的介紹了，使用一個 AD633 乘法器和三個 AD844 運算放大器，設計兩個不同類型的自動增益控制 (AGC) 電路，可以自動調整增益放大器，獲得一個穩定的數值。當輸入的信號變強，在 AGC 電路將減少增益放大器。反之，當為輸入信號削弱，AGC 的電路會增加增益放大器。由 AGC 電路實驗結果得知這項研究結果也將得到更好的回饋的反應時間及防止增益放大器,因分子為零而造成放大無限大的對策。

關鍵詞：運算放大器，自動增益控制，反向回饋

Abstract

The objective of this brief presents the implementation, using an AD633 multiplier and three AD844 operational amplifiers, of two different kinds of Automatic Gain Control (AGC) circuits which can adjust the gain of an amplifier to a stable value. As the input signal strengthens, the AGC circuits will decrease the gain of the amplifier. On the contrary, as the input signal weakens, the AGC circuits will increase the gain of the amplifier. Experimental results form two different kinds of AGC circuits, we can know this research will also improve feedback response time and prevent Af from approaching infinity as the denominator of Af tends to zero. (Af is the gain of the feedback amplifier.).

Keywords: operational amplifiers, automatic gain control, negative feedback

I. INTRODUCTION

The traditional AGC circuits are adaptive systems found in many electronic systems. The average output signal level is obtained using the negative/equivalent negative feedback concept to adjust the gain to an appropriate level for a range of input signal levels. For example, without AGC circuits the sound received by since an AM radio receiver is employed to receive signal would vary to an extreme extent from a weak signal to a strong signal; the AGC circuits effectively reduces the volume if the signal is strong and raises it when it is weak. Over the past few years, fading technique (defined as slow variations in the amplitude of the received signals) in radio circuits required continuing adjustments in the receiver's gain in order to maintain a relative constant output signal. Such situation led to the design of circuits, whose primary ideal objective was to maintain a constant signal level at the output, regardless of the signal variations at the input of the system. Normally, those circuits were described as automatic volume control circuits. A few years later they were generalized under the name of AGC circuits [1-6]. The main objective of this paper is to provide the theory and implementation of two types of the AGC circuits.

II. THEORY OF AGC CIRCUITS

The block diagram of AGC is shown in Fig. 1. The signal input from microphone or other device. The AGC maintains the output signal between the minimum and maximum thresholds. As the input signal level changes, the

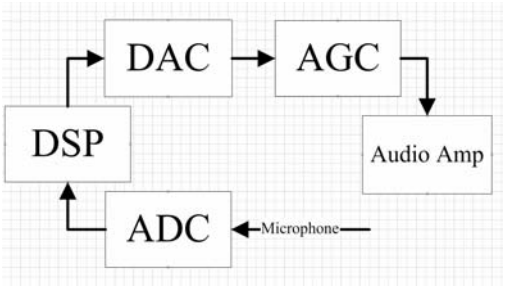

Fig. 1 Block diagram of AGC

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Manuscript received 26 September 2008; revised 12 December 2008; accepted 7 January 2009

level-controlled output may not always be the same but will always fall within the thresholds.

Let the fraction of the output that feeds back to the input be β. The voltage amplification of the feedback network determines the value of β. We design two types of AGC circuits. For the inverting type 1 (resp. non-inverting type 2) example shown in Fig. 2 (resp. Fig. 3), the feedback equation, as shown in equation (1) (resp. as shown in equation (5)), defines the closed-loop voltage gain [7] in which βA is the loop gain.

Hence, (i) for type 1 AGC diagram shown in Fig. 2

$$\frac{V_o}{V_i} = A_f = \frac{-A}{1+\beta A} \tag{1}$$

As the input voltage signal V_i suddenly increases (resp. decreases), the later output signal V_o, shown in equation (2), will decreases (resp. increases) due to the negative sign in equation (2).

$$V_O = (V_i + V_O')(-A) \tag{2}$$

Where

$$V_O' = K|V_i|V_O \tag{3}$$

Then

$$V_O = (V_i + |V_i|V_O)(-A) \tag{4}$$

In which V_o' represents the output signal of the block β .Here β is a multiplier with inputs $|V_i|$ and V_o, from the summer circle, to be decreased (resp. increased). It is the main scheme of the AGC shown in Fig. 2 for the input variation.

(ii) For type2 AGC diagram shown in Fig. 3

$$\frac{V_O}{V_i} \equiv A_f = \frac{A}{1+\beta A} \tag{5}$$

As the input voltage signal V_i suddenly increases (resp. decreases), the later output signal V_o, shown in equation (6), will increases (resp. decreases) due to the positive A in equation (6).

$$V_O = (V_i - V_O')(A) \tag{6}$$

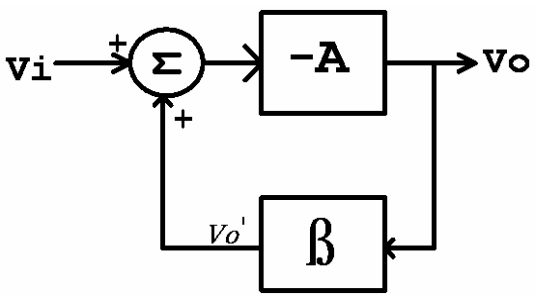


Fig. 2 Type 1 AGC diagram

where

$$V_O' = K|V_i|V_O \tag{7}$$

Then

$$V_O = (V_i - |V_i|V_O)(A) \tag{8}$$

In which V_o' represents the output signal of the block β. Here β is a multiplier with inputs $|V_i|$ and V_o, the negative feedback makes the output of the summer circle smaller (resp. larger) due to a bigger absolute value of the negative feedback signal -V_o'. It is the main scheme of the AGC shown in Fig. 3 for the input variation.

III. IMPLEMENTATIONS OF THE AGC CIRCUITS

The AD633 multiplier shown in Fig. 4 is a four-quadrant, analog multiplier. It includes the differential X and Y inputs and a summing input Z, all of which is with high input impedance. The low impedance output voltage is a nominal 10V full scale provided by a buried Zener [8].

$$W = V_O' = \frac{(x1-x2)(y1-y2)}{10} + Z = \frac{1}{10}|V_i|V_O + Z \tag{9}$$

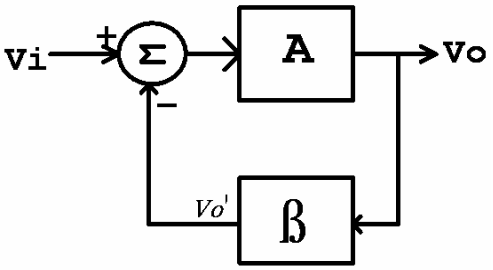


Fig. 3 Type 2 AGC diagram

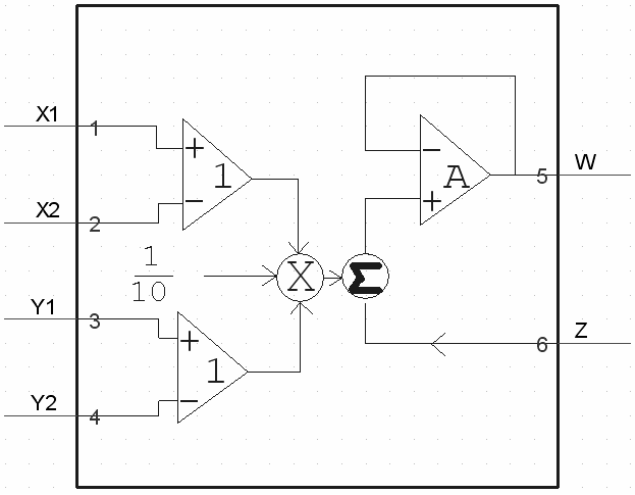


Fig. 4 AD633 multiplier

The two implementations of type 1 AGC circuits are shown in Figs. 5(a) and 5(b). The AGC circuit with a feedback amplifier structure includes the inverted operational amplifier as shown in Fig. 5(a) block A, the multiplier as shown in Fig. 5(a) U2, and the precision full-wave rectifier as shown in Fig. 5(a) block B [9]. The precision full-wave rectifier is used to get the ｜Vi｜ so that the response of time is improved and to prevent as shown in equation (1) from approaching infinity as the denominator of A_f tends to zero. In the implementation we use an AD844 for the operational amplifier and an AD633 for the multiplier [10].

Circuit analysis for the circuit shown in Fig. 5(a) gives

$$V_O = -(\frac{R_2}{R_1}V_i + \frac{R_2}{R_3}V_O') \tag{10}$$

Where

$$V_O' = \frac{1}{10}|V_i|V_O \tag{11}$$

Then

$$Av = \frac{V_O}{V_i} = \frac{\frac{-R_2}{R_1}}{1+\frac{1}{10}|V_i|\frac{R_2}{R_3}} \tag{12}$$

As shown in equation (12), if the absolute value of *Vi* decreases, then *Av* increases. In other words, if the absolute value of *Vi* is with a peak, then *Av* is with the minimum.

After analyzing the circuit shown in Fig. 5(b), we obtain.

$$V_O = -(\frac{R_2}{R_1}V_i) + (1+\frac{R_2}{R_1})V_O' \tag{13}$$

And

$$V_O' = -\frac{1}{10}|V_i|V_O \tag{14}$$

Then

$$Av = \frac{V_O}{V_i} = \frac{\frac{-R_2}{R_1}}{1+(1+\frac{R_2}{R_1})\frac{1}{10}|V_i|} \tag{15}$$

The two implementations of type 2 AGC circuits are shown in Figs. 6(a) and 6(b).The only difference between Type 1 AGC and Type 2 AGC circuits is that the former (resp. the latter) uses inverted (resp. non-inverting) type operational amplifiers.

Circuit analysis for the circuit shown in Fig. 6(a) gives

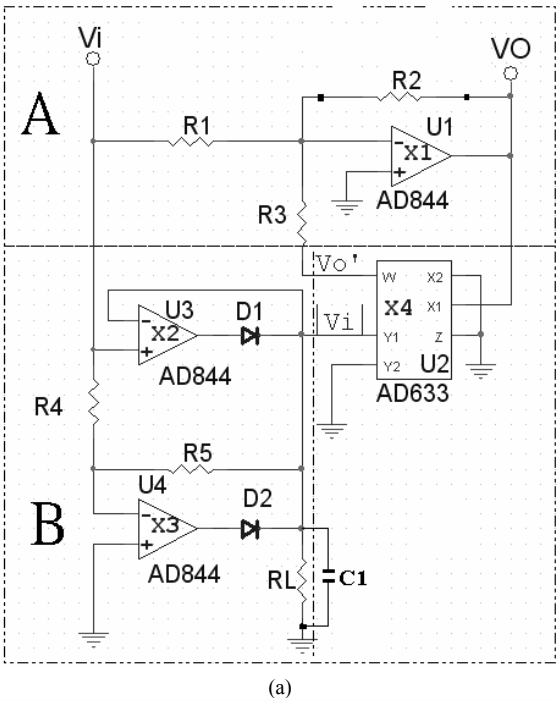
$$V_O = (1+\frac{R_2}{R_6})(\frac{R_3}{R_1+R_3}V_i + \frac{R_1}{R_{1+}R_3}V_O') \tag{16}$$

Where

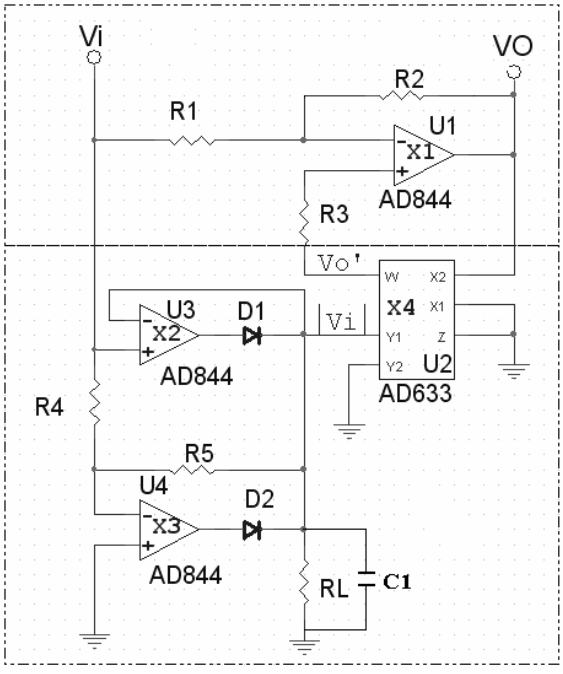
$$V_O' = -\frac{1}{10}|V_i|V_O \tag{17}$$

Then

$$Av = \frac{V_O}{V_i} = \frac{(1+\frac{R_2}{R_6})(\frac{R_3}{R_1+R_3})}{1+(1+\frac{R_2}{R_6})(\frac{R_1}{R_1+R_3})\frac{1}{10}|V_i|} \tag{18}$$



(a)



(b)

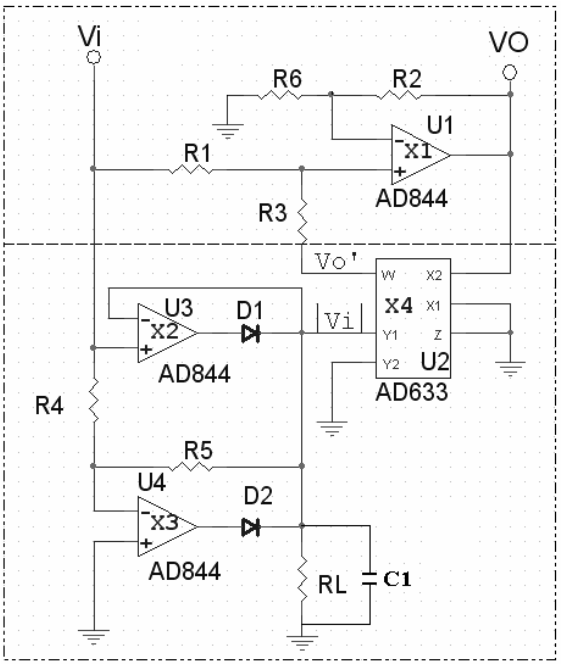
Fig. 5 (a) Type 1 AGC implementation I, (b) Type 1 AGC implementation II

After analyzing the circuit shown in Fig. 6(b), we obtain

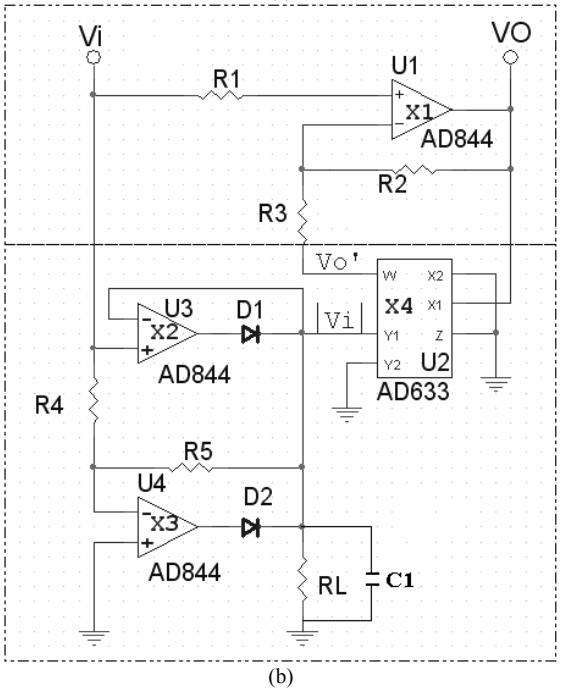
$$V_O = -(\frac{R_2}{R_3} V_O') + V_i(1+\frac{R_2}{R_3}) \tag{19}$$

Where

$$V_O' = \frac{1}{10}|V_i| V_O \tag{20}$$



(a)



(b)

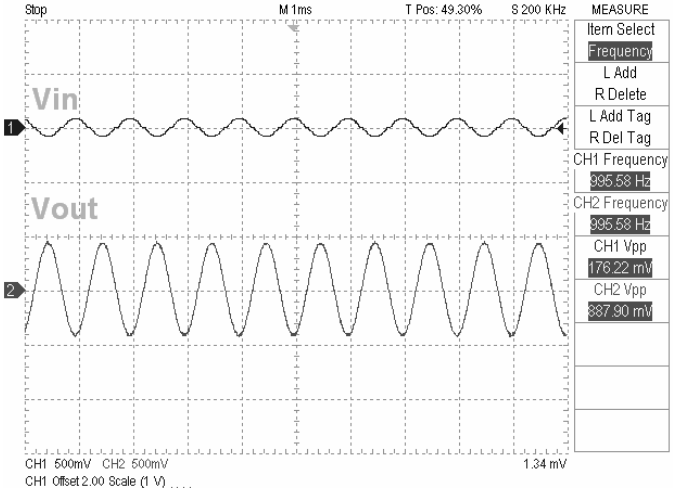
Fig. 6 (a) Type 2 AGC implementation I, (b) Type 2 AGC implementation II

Then

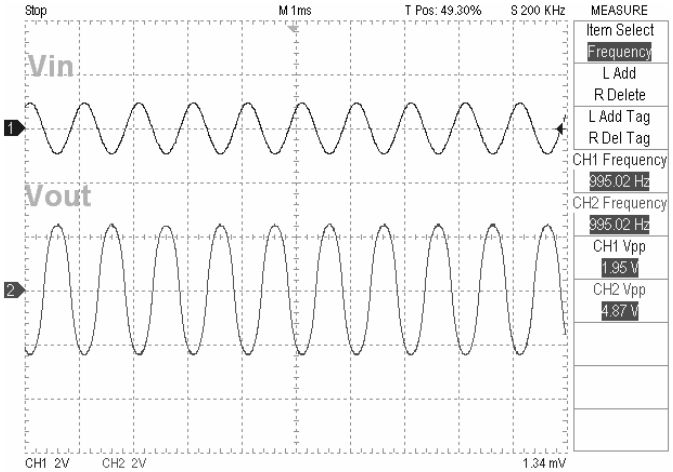
$$Av = \frac{V_O}{V_i} = \frac{(1+\frac{R_2}{R_3})}{1+\frac{R_2}{R_3}\frac{1}{10}|V_i|} \tag{21}$$

IV. EXPERIMENTAL RESULTS

Eight experimental results are shown as follows. For example, we use Fig. 5(a) type 1 AGC implementation I, the voltage supply is given by V_{DD}=12V and V_{SS}=-12V, and the component values are R_1=1KΩ±5%, R_2=5.1KΩ±5%, R_3=510Ω±5%, R_4=R_5=R_L=10KΩ±5% and C_1=100P±5%. The Vi and Vo of type 1 AGC implementation I are shown in Figs. 7(a) and 7(b).



(a)



(b)

Fig. 7 (a) Vi and Vo of Type 1 AGC implementation I (Vi p-p=176.22 mV, Vo p-p=887.90 mV, Avmin=Vo/Vi=5.0), (b) Vi and Vo of Type 1 AGC implementation I (Vi p-p=1.95 V,Vo p-p=4.87 V, Avmin= Vo/Vi=2.46)

For example, we use Fig.5 (b) type 1 AGC implementation II, the voltage supply is given by V_{DD}=12V and V_{SS}=-12V, and the component values are R_1=1KΩ±5%, R_2=5.6KΩ±5%, R_3=910Ω±5%, R_4=R_5=R_L=10KΩ±5% and C_1=100P±5%. The Vi and Vo of type 1 AGC implementation II are shown in Figs. 8(a) and 8(b).

For example, we use Fig. 6(a) type 2 AGC implementation I, the voltage supply is given by VDD=12 V and VSS=-12 V, and the component values are R_1=1KΩ±5%, R_2=5.6KΩ±5%, R_3=910Ω±5%, R_4=R_5=R_L=10KΩ±5%, R_6=510Ω±5% and C_1=100P±5%. The Vi and Vo of type 2 AGC implementation I are shown in Figs. 9(a) and 9(b).

For example, we use Fig. 6(b) type 2 AGC implementation II, the voltage supply is given by V_{DD}=12 V and V_{SS}=-12 V, and the component values are R_1=1KΩ±5%, R_2=3.9KΩ±5%, R_3=910Ω±5%, R_4=R_5=R_L=10KΩ±5% and C_1=100P±5%. The Vi and Vo of type 2 AGC implementation II are shown in Figs. 10(a) and 10(b).

For example, we use Fig.5 (b) type 1 AGC implementation II, the voltage supply is given by Vi frequency =20Hz, 10 KHz and 20 KHz, V_{DD}=12 V and V_{SS}=-12 V, and the component values are R_1=1KΩ±5%, R_2=5.6KΩ±5%, R_3=910Ω±5%, R_4=R_5=R_L=10KΩ±5% and C_1=100P±5%. The Vi and Vo of type 1 AGC implementation II are shown in Figs. 11(a), 11(b), 11(c) and 11(d).

For example, we use Fig. 6(a) type 2 AGC implementation I, the voltage supply is given by Vi frequency =20 Hz, 10 KHz and 20 KHz, VDD=12 V and VSS=-12 V, and the component values are R_1=1KΩ±5%, R_2=5.6KΩ±5%, R_3=910Ω±5%, R_4=R5=R_L=10KΩ±5%, R_6=510Ω±5% and C_1=100P±5%. The Vi and Vo of type 2 AGC implementation I are shown in Figs. 12(a), 12(b), 12(c)and 12(d).

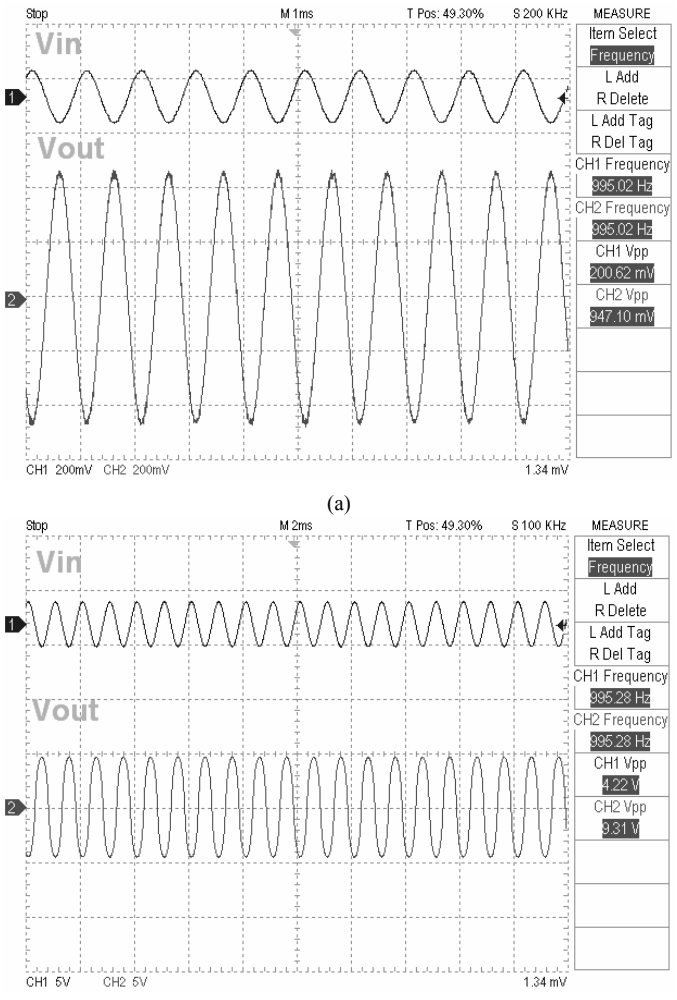


Fig. 8 (a) Vi and Vo of Type 1 AGC implementation II (Vi p-p=200.62 mV, Vo p-p=947.10 mV, Avmin=Vo/Vi=4.72), (b) Vi and Vo of Type 1 AGC implementation II (Vi p-p=4.22 V, Vo p-p=9.31 V, Avmin=Vo/Vi=2.2)

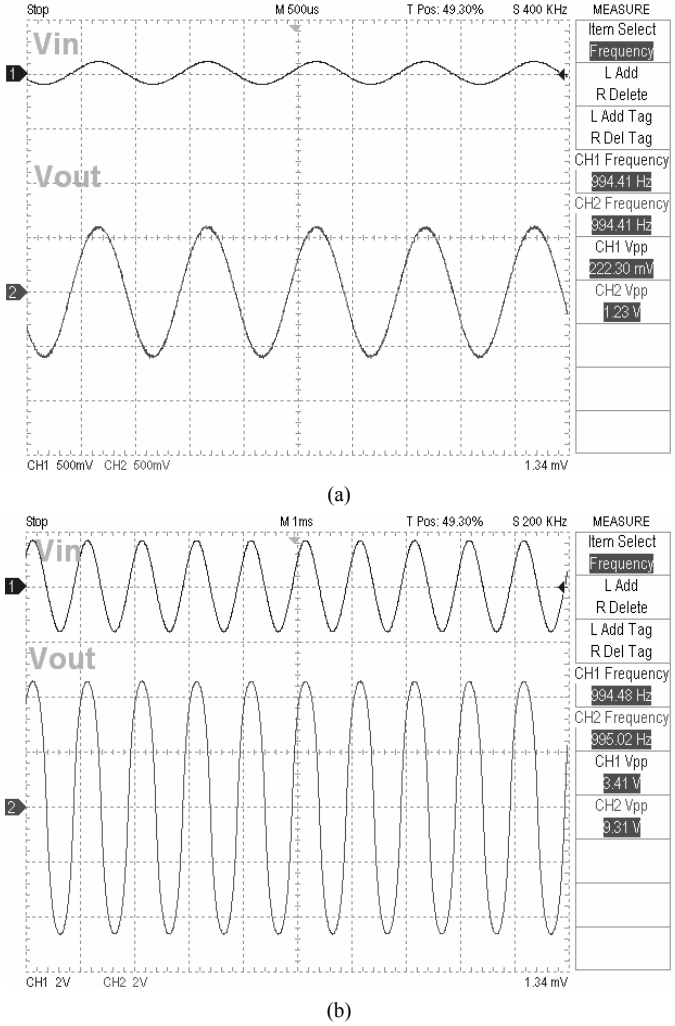
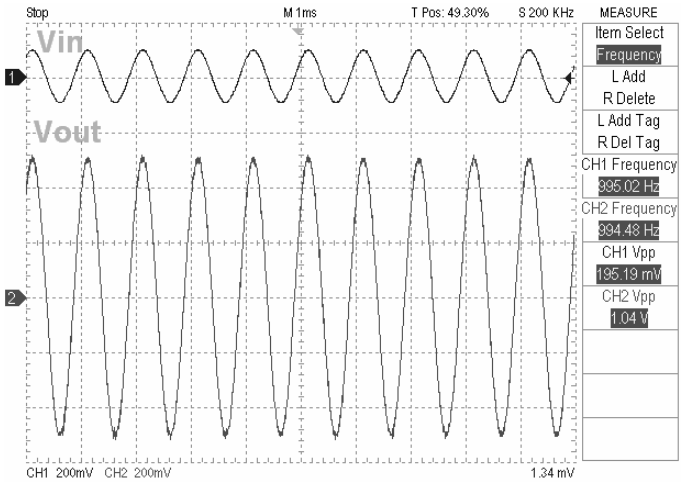


Fig. 9 (a) Vi and Vo of Type 2 AGC implementation I (Vi p-p=222.3 mV, Vo p-p=1.23 V, Avmin=Vo/Vi=5.5), (b) Vi and Vo of Type 2 AGC implementation I (Vi p-p=3.41 V,Vo p-p=9.31 V, Avmin=Vo/Vi= 2.73)

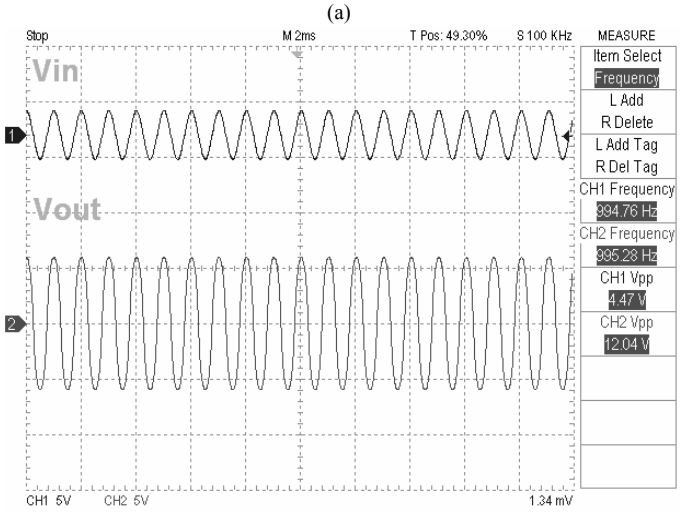
Table 1 Comparison of the Vi's and Vo's

Vi_{P-P} (V)	1.72	1.76	1.84	1.92	2.04	2.16	2.24	2.32
Vo_{P-P} (V)	6.24	6.36	6.52	6.64	6.76	6.88	6.96	6.98

For example, we use Fig. 6(a) type 2 AGC implementation I, the voltage supply is given by Vi frequency =20 Hz, 10 KHz and 20 KHz, VDD=12 V and VSS=-12 V, and the component values are R_1=1KΩ±5%, R_2=5.6KΩ±5%, R_3=910Ω±5%, R_4=R_5=R_L=10KΩ±5%, R_6=510Ω±5% and C_1=100P±5%. The Vi and Vo of type 2 AGC implementation I are shown in Table 1.

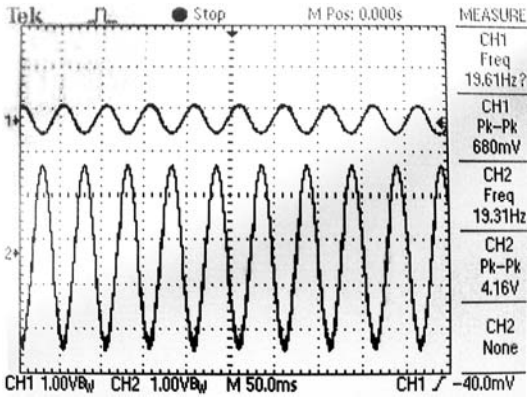


(a)

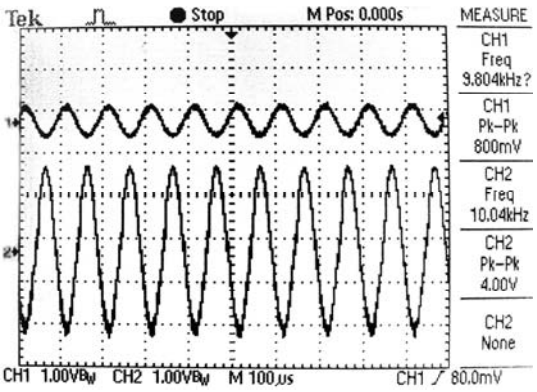


(b)

Fig. 10 (a) Vi and Vo of Type 2 AGC implementation II (Vi p-p=195.19 mV, Vo p-p=1.04 V, Avmin=Vo/Vi=6.5), (b) Vi and Vo of Type 2 AGC implementation II (Vi p-p=4.47 V, Vo p-p=12.04 V, Avmin=Vo/Vi=2.69)



(a)



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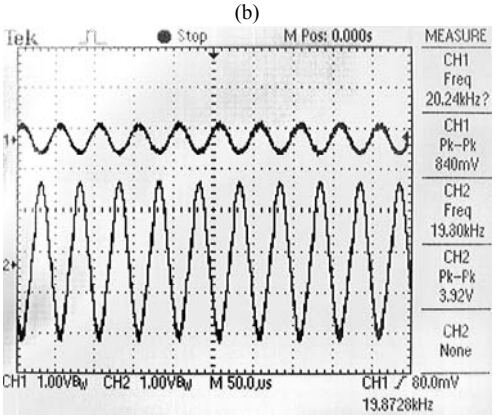
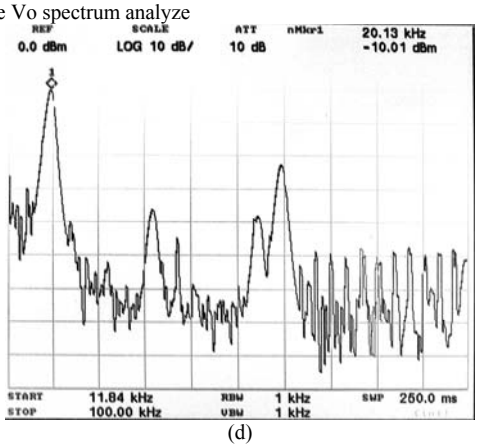


(c)

The Vo spectrum analyze



(d)

Fig. 11 (a) Input 20 Hz Signal of Type 1 AGC implementation II, (b) Input 10 KHz Signal of Type 1 AGC implementation II, (c) Input 20 KHz Signal of Type 1 AGC implementation II, (d) Input 20 KHz Signal of Type 1 AGC implementation II

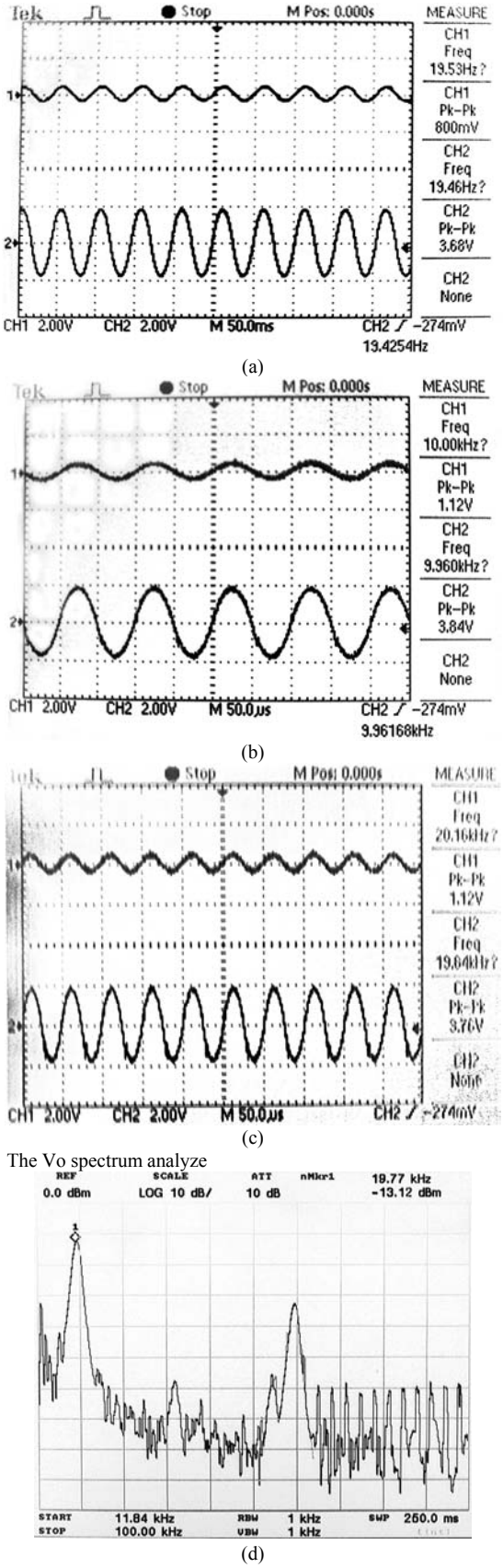


Fig. 12 (a) Input 20 Hz Signal of Type 2 AGC implementation I, (b) Input 10 KHz Signal of Type 2 AGC implementation I, (c) Input 20 KHz Signal of Type 2 AGC implementation I, (d) Input 20 KHz Signal of Type 1 AGC implementation II

Table 2 Comparison of the measured and the theoretical Vo's

Vi	Measured Vo	Theoretical Vo	Deviation %
176mV Fig. 6(a)	889.9 mV	825 mV	7.87%
1.95V Fig. 6(b)	4.87 V	5.04 V	-3.49%

From the above experiment, AGC circuits can control the output signal with the gain at a stable value when the input signal varies in magnitude.

Based upon the above experimental results, the comparison of the measured Vo and the theoretical Vo of Figs. 7(a) and 7(b) are shown in Table 2 and validates that the smaller Vi, the larger Av, and vice versa. All of the other experimental results shown in Figs. 8 to 10 are also in agreement with the same theoretical prediction.

Testing equipments used in the above experiments include the spectrum analyzer (NS-30A), the Audio analyzer (MAK-6581), the oscilloscope (Acute DS1002), and the power supply (GPC-3060D).

V. CONCLUSIONS

The AGC circuit is a part of any audio systems where a constant output signal is desired. The complexity of the AGC circuit is determined by the requirements of the audio system. Therefore the analysis, design and implementation of the AGC circuit may become quite difficult. Nonetheless, the four AGC circuits, implemented from negative or equivalent negative feedback diagrams, are presented in this paper, which can control the output signal with the gain at a stable value when the input signal varies in magnitude**.** From the above four AGC circuits can improve when the input signal a spike, is only a short period of time to achieve stability. Experimental results using the AD844 and the AD633 are also given to validate the theoretical predictions.

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